

United States Institute for Theatre Technology, Inc.

U S I T T

AMX192 ANALOG MULTIPLEX DATA TRANSMISSION STANDARD
FOR DIMMERS AND CONTROLLERS

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A Project of the USITT Engineering Commission

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AMX192 Analog Multiplex Data Transmission

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1.0 SCOPE

This Standard describes a method of analog multiplexed data transmission between controllers and dimmers. It covers electrical characteristics, data timing, connector type, and cable type.

2.0 APPLICABILITY

This Standard is intended as a guide for:

1. Equipment manufacturers and system specifiers who wish to integrate systems of dimmers and controllers utilizing analog multiplexed control.
2. Equipment manufacturers seeking to adopt a basic controller-dimmer analog multiplex data transmission protocol.

It is important to note that the origins of this Standard come from a control protocol originally developed by Strand Lighting (Strand Century Inc.). This protocol is used by a large installed base of equipment manufactured by Strand and many other manufacturers. One of the objectives of this Standard is to describe a protocol that will successfully communicate with most of this existing equipment. Because the original protocol has undergone many slightly different versions, this Standard is broken down into two major areas:

1. Receive Timing. Dimmers or other receiving devices that adhere to these timing requirements should be able to successfully communicate with most existing consoles that use different variations of the original Strand protocol.
2. Transmit Timing. Controllers or other transmitting devices that adhere to these timing requirements should be able to communicate with most existing dimmers that use the different variations of the original Strand protocol.

There are substantial differences between the receive timing and the transmit timing. New controllers adhering to this Standard must produce a signal acceptable to a wide variety of dimmers, and new dimmers must be able to listen to a number of different controller signals. As an example, note that new consoles should provide a wide "analog valid" window, but new dimmers must be able to cope with the differences in existing consoles and use a narrow "sample window". These differences in timing between the Receive Standard and the Transmit Standard produce enough tolerance to cover worst case variations on the original Strand protocol.

Although widespread adoption of this Standard is sought by USITT, compliance with the Standard is strictly voluntary. Furthermore, it is not intended as a replacement for existing protocols already manufactured, but rather as an addition to existing protocols which will broaden the installed base of controllers and dimmers that can communicate with each other.

3.0 CROSS REFERENCE

See EIA Standards RS-422A and RS-485 available from:
Electronic Industries Association
Standards Sales Office
2001 Eye Street NW
Washington, D.C. 20006
202-457-4900

4.0 TRANSMISSION MEDIUM

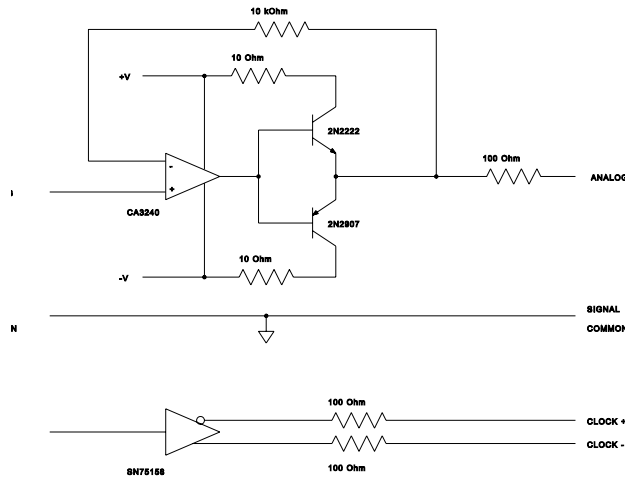
Data transmission shall be via a four conductor control cable with conductors designated as follows:

- ANALOG LEVEL
- SIGNAL COMMON
- DIFFERENTIAL CLOCK TRUE (CLOCK +)
- DIFFERENTIAL CLOCK COMPLEMENT (CLOCK -)

Analog dimmer control levels shall be time multiplexed on the ANALOG line, referenced to the SIGNAL COMMON line. These levels shall vary from 0 to +5 VDC representing dimmer output levels from 0 to 100%. Synchronization of the controller (transmitting device) and the dimmer (receiving device) shall be via clock pulses on the DIFFERENTIAL CLOCK TRUE and DIFFERENTIAL CLOCK COMPLEMENT.

5.0 DRIVER ELECTRICAL CHARACTERISTICS

See Figure 1 for a description of differential clock driver and analog driver circuits. It is strongly recommended that these circuits be utilized in order to insure compatibility with existing equipment.



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Figure 1 - AMX192 Recommended Drivers

5.1 DRIVER PARAMETERS

PARAMETER	MIN	TYP	MAX	UNIT
Vf "Full" analog level	4.9	5.0	5.1	Vdc
Vo "Off" analog level	0.0	0.0	0.1	Vdc
Ro Analog Driver output impedance		100		ohms
Maximum analog driver safe short circuit duration	unlimited			
Vhi Differential Clock - Hi level		4.0		Vdc
Vlo Differential Clock - Low level		1.0		Vdc
Ros Clock Driver output impedance		100		ohms

Note: Differential clock driver shall conform to RS-422A specifications and be connected to the line through 100 ohm series resistors. Above voltage and impedance values for the clock driver are for reference only.

6.0 RECEIVER ELECTRICAL CHARACTERISTICS

See Figure 2 for a description of recommended analog and differential clock receiver circuits. It is strongly recommended that these circuits be utilized in order to insure compatibility with existing equipment. In cases where no more than four receivers will be connected to the data link, use of Standard RS-422A receivers shall be permitted.

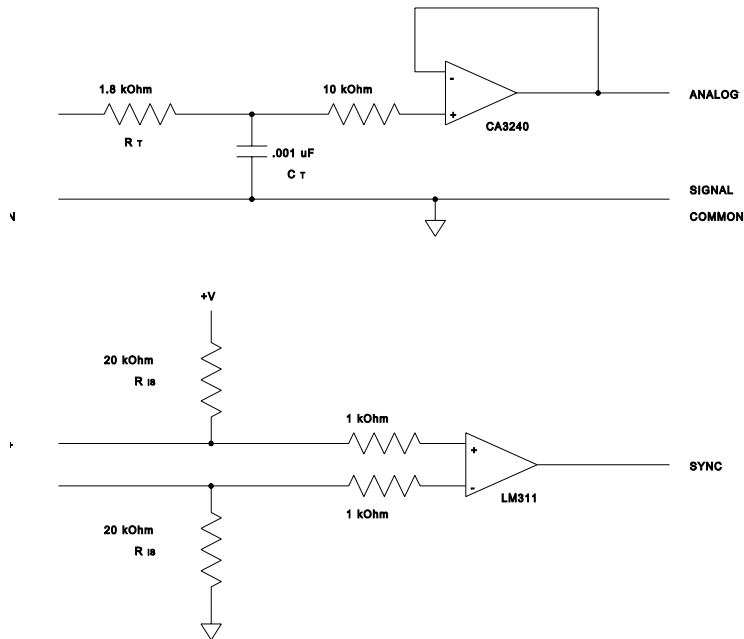


Figure 2 - AMX192 Recommended Receivers

6.1 RECEIVER PARAMETERS

PARAMETER	MIN	TYP	MAX	UNIT
Vf "Full" analog level	4.9	5.0	5.1	Vdc
Vo "Off" analog level	0.0	0.0	0.1	Vdc
Rt Analog receiver termination, per dimmer		20		Kohm
Ris Clock receiver termination, per dimmer		240		Kohm

Note: The above termination values for Rt and Ris allow the system designer to calculate the ideal termination for systems with fixed numbers of receivers with fixed numbers of receivers and dimmers. In cases where system size is not fixed, it is acceptable to under terminate the line, but Rt should be 1.8 Kohm minimum and Ris should be 20 Kohm minimum. In no case should the line termination be reduced below that of 192 dimmers using the per dimmer values in the table above.

6.2 MAXIMUM NUMBER OF RECEIVERS PER DATA LINK

The maximum number of receivers per data link shall be 16 when using the type specified in Figure 2. When using Standard RS-422A receivers, the maximum number shall be four per data link.

7.0 TRANSMIT TIMING

See Figure 3 for a diagram of Transmit Timing. Timing Parameters for this diagram are as follows:

PARAMETER	MIN	TYP	MAX	UNIT
The following parameters define the "analog valid" window. Analog level should be output no later than the leading edge of the SYNC pulse, and should be maintained for at least 50 μ Seconds.				
Trs RESET Pulse Duration	35	40	70	μ Sec
Tri Reset Interframe delay after RESET pulse trailing edge	15			μ Sec
Ts Dimmer SYNC pulse duration	6	8	10	μ Sec
Ta Advance of valid analog level before SYNC pulse leading edge	0			μ Sec
Th Valid analog level hold from leading edge of SYNC pulse	50			μ Sec

The following parameters define the refresh cycle. Minimum refresh cycle is a function of the number of dimmer frames transmitted, up to a maximum of 192. There is no minimum time between the start of the last dimmer frame and the start of the next RESET frame.

PARAMETER	MIN	TYP	MAX	UNIT
Tc 192 dimmer refresh cycle	10	50	500	mSec
Td Dimmer frame duration	50			μ Sec

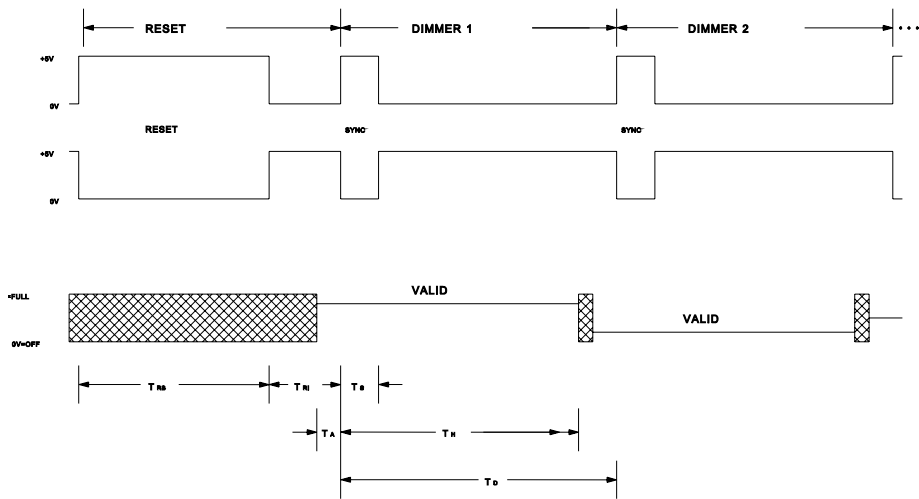


Figure 3 - AMX192 Transmit Timing Diagram

8.0 RECEIVE TIMING

See Figure 4 for a diagram of Receiving Timing. Parameters for this diagram shall be as follows:

PARAMETER _____ MIN _____ TYP _____ MAX _____ UNIT _____
 The following parameters define the analog "sample window" from 20 to 50 μ Seconds after the leading edge of the SYNC pulse:

Trs	RESET pulse durations	30	40	70	μ Sec
Tri	RESET interframe delay after RESET pulse trailing edge	10			μ Sec
Tav	Analog Valid delay after dimmer SYNC pulse leading edge	3	8	15	μ Sec
Th	Hold of valid analog level from leading edge of dimmer SYNC pulse	50			μ Sec

The following parameters define the refresh cycle. Minimum refresh cycle is a function of the number of dimmer frames transmitted, up to a maximum of 192. There is no minimum time between the start of the last dimmer frame and the start of the next RESET frame. Dimmers must be able to accept a lapse in transmission for up to 500 milliseconds.

Tc	192 dimmer refresh cycle	10	50	500	mSec
Td	Dimmer frame duration	50			μ Sec

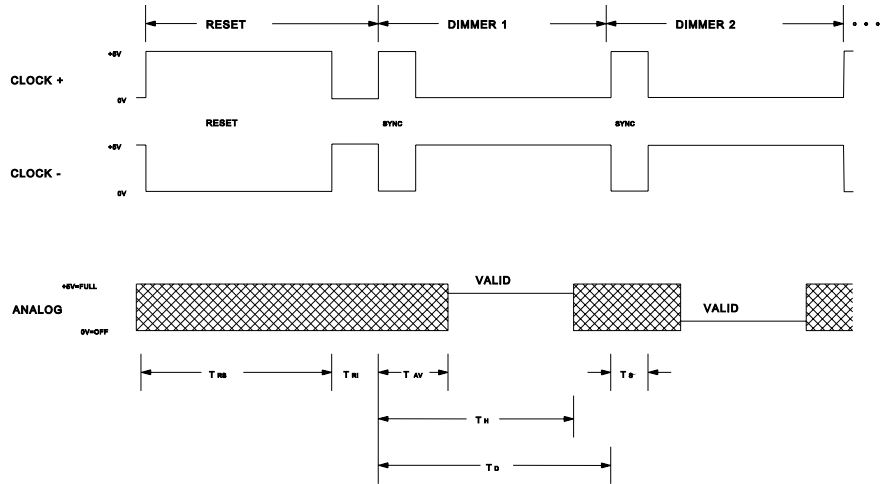


Figure 4 - AMX192 Receive Timing Diagram

9.0 NUMBER OF DIMMERS PER DATA LINK

Each data link shall support up to 192 dimmers. Multiple links shall be used where larger numbers of dimmers are required. Since a RESET pulse can occur after any valid dimmer frame, there is no minimum number of dimmers per data link.

10.0 CONNECTORS

Where connectors are used, the data link shall utilize 4-pin "XLR" style microphone connectors. Some manufacturers of these connectors are:

- Switchcraft
- ITT Cannon
- Neutrik

Optionally, when mating with existing Strand equipment, Switchcraft "Mini Connectors" (typical part numbers TY4F, TA4ML, and TA4FL) may be utilized.

10.1 CONNECTOR SEX

Where "XLR" style connectors are utilized, male connectors shall be utilized on controllers or other transmitting devices and female connectors shall be utilized on dimmers and other receiving devices.

Where "Mini Connectors" are utilized, all equipment shall utilize female connectors and all cables shall utilize male connectors except for specific "extension" cables, which shall be male-female.

10.2 CONNECTOR PIN DESIGNATION

"XLR" Connector Pin Designations shall be as follows:

PIN 1 - Signal Common
PIN 2 - Differential Clock True (Clock +)
PIN 3 - Analog Level
PIN 4 - Differential Clock Complement (Clock -)

"Mini Connector" Pin designations shall be as follows:

PIN 1 - Differential Clock Complement (Clock -)
PIN 2 - Signal Common
PIN 3 - Differential Clock True (Clock +)
PIN 4 - Analog Level

11.0 CABLE

Recommended cable shall be Belden 9156 or equivalent which utilizes two unshielded 18 AWG twisted pairs.

11.1 MAXIMUM LENGTH

Maximum Cable length shall be 1000 feet from controller to last dimmer unit connected to the data link.

11.2 CABLE INSTALLATION AND ROUTING

Where permanently installed, cable shall be routed through metal conduit containing no AC power conductors which might cause induced interference.

12.0 MARKING AND IDENTIFICATION

Equipment conforming to this Standard may be marked and identified with "USITT AMX192" or "AMX192".

Compliance with this Standard is the responsibility of the manufacturer, and such marking and identification does not constitute certification or approval by the USITT.

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